REMARKS

Claims 1-32 were pending in the Application. Applicant cancels claims 22-32 without prejudice or disclaimer to further prosecution and not in response to prior art. Hence, claims 1-21 are pending in the Application.

Claims 1, 8, 16 and 22 are objected to. Claim 28 is rejected under 35 U.S.C. §112, second paragraph. Claims 1-3, 5-8, 10-17, 20 and 22-28 are rejected under 35 U.S.C. §102(b). Claims 1-3, 7, 16-17, 20-28 and 30 are rejected under 35 U.S.C. §102(e). Claims 4, 9, 18-19, 21 and 30 are rejected under 35 U.S.C. §103(a). Applicant respectfully traverses these rejections for at least the reasons stated below and respectfully requests the Examiner to reconsider and withdraw these rejections.

I. ELECTIONS/RESTRICTIONS:

Applicant affirms the election of Group 1, claims 1-28 and 30, without traverse. Applicant acknowledges that claims 29 and 31-32 are withdrawn from further consideration by the Examiner.

II. INFORMATION DISCLOSURE STATEMENT:

Applicant submits herewith a new information disclosure statement that includes a smaller, more relevant listing of documents per your request.

III. CLAIM OBJECTIONS:

The Examiner objects to claims 1, 8 and 16 because each paragraph begins with a capital letter. Office Action (3/23/2006), page 4. Applicant amended claims 1, 8 and 16 accordingly as indicated above. Applicant respectfully requests the Examiner to withdraw the objections to claims 1, 8 and 16.

IV. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH:

The Examiner rejects claim 28 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant cancelled claim 28 and

hence the rejection to claim 28 is moot.

V. REJECTIONS UNDER 35 U.S.C. §102(b):

The Examiner has rejected claims 1-3, 5-8, 10-17 and 20 under 35 U.S.C. §102(b) as being anticipated by Mathur (U.S. Patent No. 6,424,658). Applicant respectfully traverses these rejections for at least the reasons stated below and respectfully requests the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicant respectfully asserts that Mathur does not disclose "an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claim 16. The Examiner cites packets 3 and 6 in Figure 9 as well as column 1 in Figure 9 of Mathur as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 6. Applicant respectfully traverses.

Mathur instead discloses that in the example of Figure 9, the packet memory is divided into several regions, one for each input port. Column 11, lines 37-38. Mathur further discloses that the output ports are not assigned any memory space. Column 11, lines 38-39. Mathur further discloses that the region for port A includes rows 1, 2, 3, 4, while the region for port C contains rows 34, 35, 36, 37. Column 11, lines 39-41. Mathur further discloses that packet 1 received by port A is written into row 1. Column 11, line 44. Mathur further discloses that since this is a small packet of 64 bytes, it occupies only the first two columns and the other 46 columns in row 1 are not used. Column 11, lines 44-46. Mathur further discloses that packet 3 occupies the entire row 3, all 48 columns. Column 11, lines 49-50. Hence, as illustrated in Figure 9, Mathur discloses dividing the packet memory into regions corresponding to each input port. Each region includes multiple rows that are allocated to store data from a particular input port. Further, each row includes 48

columns in which all or a portion of the columns may be used to store the data received from the associated input port.

There is no language in the passages that describe Figure 9 that discloses a shared memory that includes an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width. Instead, Mathur discloses 48 columns for each row where all or a portion of the columns may be used to store the data received from the associated input port. Thus, Mathur does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16. The Examiner cites column 2, line 55 – column 3, line 11; column 3, lines 31-44; column 5, lines 56-61; column 11, lines 44-56 and Figures 6 and 7 of Mathur as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 6. Applicant respectfully traverses.

Mathur instead discloses that the memory must have a bandwidth of 200 M bytes/sec for a non-blocking switch with just 8 ports. Column 2, lines 58-59. Mathur further discloses that a very fast memory with a 10-nanosecond access time must have a data-bus width of nearly 100 bits to meet such a bandwidth requirement. Column 3, lines 6-8. Mathur further discloses that although graphics controllers are in a different technical field than network switches, the inventor has realized that such embedded DRAM technology could solve performance and cost problems for network switches. Column 3, lines 36-39. Mathur further discloses that when packets are aligned to DRAM pages, the inventor has realized that only the DRAM row address where the packet is stored needs to be sent to the receiving port. Column 5, lines 56-58. Mathur further discloses that since this is a small packet of 64 bytes, it

occupies only the first two columns and the other 46 columns in row 1 are not used. Column 11, lines 44-46. Mathur further discloses that packet 3 occupies the entire row 3, all 48 columns. Column 11, lines 49-50.

There is no language in the cited passages that discloses circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width. Neither is there any language in the cited passages that discloses circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width during a first time period. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width from the selected row. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width from the selected row during a second time period. Neither is there any language in the cited passages that discloses reading the selected data as a word of the predetermined word-width from the selected row during a second time period for output at the second one of the ports. Thus, Mathur does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words" as recited in claim 8. The Examiner cites column 6, lines 36-65 of Mathur as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 6. Applicant respectfully traverses and asserts that Mathur instead discloses that port A logic and port B logic are bi-directional, each having a receive first-in-first-out FIFO and a transmit FIFO that connects to a twisted pair through physical-layer transceivers. Column 6, lines 33-36. Hence, Mathur discloses that the ports include FIFO buffers. There is no language in the cited passage that discloses a buffer

associated with each of the ports. Neither is there any language in the cited passage that discloses a buffer associated with each of the ports for assembling a stream of data words. Neither is there any language in the cited passage that discloses a buffer associated with each of the ports for assembling a stream of data words being input into the switch into a single word of a predetermined width. Neither is there any language in the cited passage that discloses a buffer associated with each of the ports for assembling a stream of data words being input into the switch into a single word of a predetermined width and for converting single data words of the predetermined width being output from the switch into a stream of data words. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "a shared-memory for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width and circuitry for selecting a said row in response to a received address" as recited in claim 8. The Examiner cites packets 3 and 6 in Figure 9 as well as column 1 in Figure 9 of Mathur as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 6. Applicant respectfully traverses.

Mathur instead discloses that in the example of Figure 9, the packet memory is divided into several regions, one for each input port. Column 11, lines 37-38. Mathur further discloses that the output ports are not assigned any memory space. Column 11, lines 38-39. Mathur further discloses that the region for port A includes rows 1, 2, 3, 4, while the region for port C contains rows 34, 35, 36, 37. Column 11, lines 39-41. Mathur further discloses that packet 1 received by port A is written into row 1. Column 11, line 44. Mathur further discloses that since this is a small packet of 64 bytes, it occupies only the first two columns and the other 46 columns in row 1 are not used. Column 11, lines 44-46. Mathur further discloses that packet 3 occupies the entire row 3, all 48 columns. Column 11, lines 49-50. Hence, as

illustrated in Figure 9, Mathur discloses dividing the packet memory into regions corresponding to each input port. Each region includes multiple rows that are allocated to store data from a particular input port. Further, each row includes 48 columns in which all or a portion of the columns may be used to store the data received from the associated input port.

There is no language in the cited passages that discloses a shared-memory for effectuating a transfer of data from a first one of the ports to a second one of the ports through corresponding ones of the buffers. Neither is there any language in the cited passages that discloses a shared-memory comprising a plurality of banks[1]. Neither is there any language in the cited passages that discloses a shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width. Neither is there any language in the cited passages that discloses a shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of the predetermined width and circuitry for selecting a row in response to a received address. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks" as recited in claim 8. The Examiner cites column 9, lines 8-25 of Mathur as disclosing the above-cited claim limitations. Office Action (3/23/2006), page 6. Applicant respectfully traverses and asserts that Mathur instead discloses that the input-port table is a memory allocation table with one entry for each row of the packet memory allocated to the port. Column 9, lines 8-10. Mathur

[1] The Examiner appears to be asserting that each row of the packet memory is considered to be a bank. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that each row of the packet memory, as disclosed in Mathur, is a bank. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that it would have been recognized by persons of ordinary skill that each row of the packet memory, as disclosed in Mathur, is a bank. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

further discloses that each entry contains the row address and a free/busy bit. Column 9, line 10. Hence, Mathur discloses a single table that contains entries containing row addresses. There is no language in the cited passage that discloses a plurality of available address tables each for maintaining a queue of addresses available for writing the single words of data. Neither is there any language in the cited passage that discloses a plurality of available address tables each for maintaining a queue of addresses available for writing the single words of data to a corresponding one of the banks. Neither is there any language in the cited passage that discloses a plurality of used address tables each for maintaining a queue of addresses for reading. Neither is there any language in the cited passage that discloses a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of the banks. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by Mathur. M.P.E.P. §2131.

Claims 2-3 and 5-6 each recite combinations of features of claim 1, and thus are not anticipated by Mathur for at least the above-stated reasons. Claims 10-15 each recite combinations of features of claim 8, and thus are not anticipated by Mathur for at least the above-stated reasons. Claims 17 and 20 each recite combinations of features of claim 16, and thus are not anticipated by Mathur for at least the above-stated reasons. Claims 2-3, 5-6, 10-15, 17 and 20 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Mathur.

For example, Mathur does not disclose "a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width" as recited in claim 2 and similarly in claim 17. The Examiner cites column 6, lines 36-65 of Mathur as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 6. Applicant respectfully traverses and asserts that Mathur instead discloses that port A logic and port B logic are bi-directional, each having a receive first-in-first-out FIFO and a transmit FIFO that connects to a twisted pair through physical-layer transceivers. Column 6, lines 33-36. Hence, Mathur discloses that the ports includes FIFO buffers. However, claims 2 and 17 do not recite a port that

comprises a buffer. Instead, claims 2 and 17 recite a buffer associated with each port. Neither is there any language in the cited passage that discloses a buffer associated with each port for converting words of data from an initial bit-width to the predetermined bit width. Thus, Mathur does not disclose all of the limitations of claims 2 and 17, and thus claims 2 and 17 are not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead" as recited in claim 3. The Examiner has not specifically addressed this claim limitation. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Mathur as allegedly disclosing the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 3. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "a used addressed table for storing addresses already used for writing data to selected rows in said array" as recited in claim 6. The Examiner cites column 9, lines 8-25 of Mathur as disclosing the above-cited claim limitations. Office Action (3/23/2006), page 6. Applicant respectfully traverses and asserts that Mathur instead discloses that the input-port table is a memory allocation table with one entry for each row of the packet memory allocated to the port. Column 9, lines 8-10. Mathur further discloses that each entry contains the row address and a free/busy bit. Column 9, line 10. Hence, Mathur discloses a table that contains entries containing row addresses. There is no language in the cited passage that discloses a table for storing addresses already used for writing data. Neither is there any language in the cited passage that discloses a table for storing addresses already used for writing data to selected rows in the array. Thus, Mathur does not disclose all of the limitations of claim 6, and thus claim 6 is not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "wherein each of said plurality of available address tables comprises a first-in-first-out memory" as recited in claim 10. The Examiner states that "the input port table in Mathur operates as a FIFO as recited." Office Action (3/23/2006), page 6. Applicant respectfully traverses and asserts that there is no language in Mathur[2] that discloses that input-port table (element 60) in Mathur comprises a FIFO memory as asserted by the Examiner. Thus, Mathur does not disclose all of the limitations of claim 10, and thus claim 10 is not anticipated by Mathur. M.P.E.P. §2131.

Applicant further asserts that Mathur does not the limitations of claims 11-15. The Examiner has not specifically addressed these claim limitations. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Mathur as allegedly disclosing the claim limitations of claims 11-15, the Examiner has not established a *prima facie* case of anticipation in rejecting claims 11-15. M.P.E.P. §2131.

Applicant further asserts that Mathur does not disclose "wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment" as recited in claim 20. The Examiner has not specifically addressed this claim limitation. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Mathur as allegedly disclosing the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 20. M.P.E.P. §2131.

[2] Column 9, lines 1-16 of Mathur discuss the input port table.

As a result of the foregoing, Applicant respectfully asserts that each and every claim limitation was not found within Mathur, and thus claims 1-3, 5-8, 10-17 and 20 are not anticipated by Mathur. M.P.E.P. §2131.

VI. REJECTIONS UNDER 35 U.S.C. §102(e):

The Examiner has rejected claims 1-3, 7, 16-17 and 20-21 under 35 U.S.C. §102(e) as being anticipated by Curtis et al. (U.S. Patent No. 6,925,086) (hereinafter "Curtis"). Applicant respectfully traverses these rejections for at least the reasons stated below and respectfully requests the Examiner to reconsider and withdraw these rejections.

As stated above, for a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicant respectfully asserts that Curtis does not disclose "an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claim 16. The Examiner cites column 1, lines 45-52; column 4, lines 19-29 and Figures 1, 3 and 6 of Curtis as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 7. Applicant respectfully traverses and asserts that Curtis instead discloses a packet memory system that includes a memory cell array for storing a predefined number of packets. Column 1, lines 46-48. Curtis further discloses that each packet includes a pre-determined number of segments. Column 1, lines 48-49. Curtis further discloses that each of the segments defines a starting point of a memory access. Column 1, lines 49-50. Curtis further discloses a cache line packet broken into four segments A, B, C and D. Column 4, lines 19-21. Curtis further discloses a memory cell array (element 102) that allows a device to read or write one cell after another and allows it to stop a burst at any point along the way. Column 2, lines 55-57. There is no language in the cited passages that discloses that the memory cell array of Curtis (Applicant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) is arranged as a plurality of rows and a single

column having a width equal to a predetermined word-width. Thus, Curtis does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Curtis. M.P.E.P. §2131.

Applicant further asserts that Curtis does not disclose "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16. The Examiner cites column 2, lines 38-43; column 3, line 63 – column 4, line 18; and Figure 4 of Curtis as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 7. Applicant respectfully traverses.

Curtis instead discloses a packet memory system including a memory cell array having, for example, M rows by N 32 bit dynamic random access memory (DRAM) cells. Column 2, lines 38-40. Curtis further discloses a switch data flow that includes a plurality of ports. Column 3, lines 65-67. Curtis further discloses a timing diagram illustrating operation of the packet memory system of the preferred embodiment as compared to the operation of a conventional DDR II system. Column 4, lines 7-10. There is no language in the cited passages that discloses that the memory cell array of Curtis (Applicant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for writing selected data presented at the first one of the ports to a selected row in the array. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis (Applicant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined word-width during a first time period. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis (Applicant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for reading the selected data as a word of the pre-determined word-width from the selected row. Neither is there any language in the cited passages that

discloses that the memory cell array of Curtis (Applicant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for reading the selected data as a word of the pre-determined word-width from the selected row during a second time period. Neither is there any language in the cited passages that discloses that the memory cell array of Curtis (Applicant assumes that the Examiner is citing to element 100 of Curtis as disclosing a shared memory) includes circuitry for reading the selected data as a word of the pre-determined word-width from the selected row during a second time period for output at the second one of the ports. Thus, Curtis does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Curtis. M.P.E.P. §2131.

Claims 2-3 and 7 each recite combinations of features of claim 1, and thus are not anticipated by Curtis for at least the above-stated reasons. Claims 20-21 each recite combinations of features of claim 16, and thus are not anticipated by Curtis for at least the above-stated reasons. Claims 2-3, 7 and 20-21 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Curtis.

For example, Curtis does not disclose "a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width" as recited in claim 2 and similarly in claim 17. The Examiner cites Figure 1 of Curtis as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 7. Applicant respectfully traverses and asserts that Curtis instead discloses a packet memory system including a memory cell array having, for example, M rows by N 32 bit dynamic random access memory (DRAM) cells. Column 2, lines 38-40. There is no language in Curtis that discloses a buffer associated with each port. Neither is there any language in Curtis that discloses a buffer associated with each port for converting words of data from an initial bit-width to a predetermined bit width. Thus, Curtis does not disclose all of the limitations of claims 2 and 17, and thus claims 2 and 17 are not anticipated by Curtis. M.P.E.P. §2131.

Applicant further asserts that Curtis discloses "wherein said predetermined

bit-width is equal to a bit-width of certain bit width and associated overhead" as recited in claim 3. The Examiner cites Figure 3 of Curtis as disclosing the above-cited claim limitation. Office Action (3/23/2006), page 8. Applicant respectfully traverses. Applicant could not find any language discussing Figure 3 or any depiction in Figure 3 that discloses that the predetermined bit-width is equal to a bit-width of certain bit width and associated overhead. Thus, Curtis does not disclose all of the limitations of claim 3, and thus claim 3 is not anticipated by Curtis. M.P.E.P. §2131.

Applicant further asserts that Curtis does not disclose "wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment" as recited in claim 20. Applicant further asserts that Curtis does not disclose "where the data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), Rambus™, and programmable bit burst length interfaces" as recited in claim 21 The Examiner has not specifically addressed these claim limitations. A claim is anticipated only if each and every claim element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not cited to any passage in Curtis as allegedly disclosing the claim limitations of claims 20-21, the Examiner has not established a *prima facie* case of anticipation in rejecting claims 20-21. M.P.E.P. §2131.

As a result of the foregoing, Applicant respectfully asserts that each and every claim limitation was not found within Curtis, and thus claims 1-3, 7, 16-17 and 20-21 are not anticipated by Curtis. M.P.E.P. §2131.

VII. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner rejects claims 4, 9, 18-19 under 35 U.S.C. §103(a) as being unpatentable over Mathur, or alternatively, over Curtis. The Examiner further rejects claims 21 and 30 under 35 U.S.C. §103(a) as being unpatentable over Mathur.

Applicant respectfully traverses for at least the reasons stated below and respectfully requests the Examiner to reconsider and withdraw the rejections.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention may often be found in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that neither Mathur nor Curtis teach the claim limitations of claims 4, 9, 18, 19 and 21. Office Action (3/23/2006), page 9. However, the Examiner does not provide a motivation for modifying either Mathur or Curtis to include such limitations. The Examiner simply states:

> Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add any of these elements, because they and their advantages were widely known at the time. Office Action (3/23/2006), page 9.

This (simply stating "advantages were widely known at the time") is not a motivation for modifying Mathur or Curtis to include the above-mentioned

limitations. The Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Mathur or Curtis to include the above-mentioned limitations. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner is instead relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Since the Examiner has not provided a motivation for modifying Mathur or Curtis to include the above-mentioned limitations, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 4, 9, 18, 19 and 21. *Id.*; M.P.E.P. §2143.

Further, the Examiner states:

> Each of these limitations were obvious and well known at the time of the invention. The specific bit widths recited fall with the envisioned embodiments of a clearly scalable bit size. Advantages of using ATM format were notoriously well known. Interfaces such as DDR were widely known to have performance benefits. Strobing on both clock edges is akin to DDR and was known to improve performance. Office Action (3/23/2006), page 9.

Applicant respectfully traverses the assertion that the limitations of claims 4, 9, 18-19 and 21 are well known. In particular, Applicant respectfully traverses the assertion that having an initial bit width of 48 bits and a predetermined bit-width of 384 bits, as recited in claim 4, is well known in the art. Applicant further traverses the assertion that having streams of data words comprising eight forty-eight bit words of ATM data and having single words having a predetermined width of 384 bits, as recited in claim 9, are well known in the art. Applicant further traverses the assertion that the selected digital format that includes an asynchronous transfer mode digital data format, as recited in claim 18, is well known in the art. Applicant further traverses the assertion that having the predetermined word-width equal a bit-width of a user data portion of an asynchronous transfer mode information packet, as recited in claim 19, is well known in the art. Applicant further traverses the assertion that having a data interface selected from a group consisting of DDR, QDR, Rambus™, and programmable bit burst length interfaces, as recited in claim 21, is well known in the art. Applicant respectfully requests the Examiner to provide a reference that

teaches each of the above-cited claim limitations pursuant to M.P.E.P. §2144.03.

VIII CONCLUSION:

As a result of the foregoing, it is asserted by Applicant that claims 1-21 in the Application are in condition for allowance, and Applicant respectfully requests an allowance of such claims. Applicant respectfully requests that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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Date: June 1, 2006

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